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EXAMINER	
STAMPF, TIMOTHY R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/742,224	Applicant(s) FANG ET AL.	
	Examiner Timothy R. Stampf	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 22 December 2000.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The specification is objected to because of the following informalities.

(a) The abstract of the disclosure is objected to because it contains more than 150 words. Correction is required.

(b) The specification uses the word -- consult -- on numerous occasions in an awkward and unclear manner. For example, on page 3, lines 17-26, the word -- consult -- is used three times in reference to a formula, experience and relation. It is unclear how a formula, experience or relation can be "consulted". Similar situations occur on pages 5, 6, 8 and 9 lines 5, 17, 20 and 27, respectively. The entire specification should be checked to ensure all occurrences of the word -- consult -- are corrected.

(c) The specification refers to Fig. 4D on page 12, line 4. Fig. 4D does not exist.

(d) The entire specification should be checked to ensure that proper idiomatic English is used. For example, the Abstract, on line 25, contains the phrase -- circuit is fail before the knee point --; page 2, line 28, contains the phrase -- the difference between the difference between --; page 10, line 27, contains the phrase -- "try and error" --; page 11, line 15, contains the phrase -- an optimizating process --.

Appropriate correction is required.

Claim Objections

2. Claim 2, 9, 10 are objected to because of the following informalities:

(a) With regard to claim 2, the phrase -- in according to -- is awkward.

(b) With regard to claims 9 and 10, the phrases -- to let a last square error between said failure rate testing time relation and said testing time function is minimized --, and -- to let an error between said failure rate testing time relation and said testing time function is minimized -- is awkward.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 1, 12 and 19 (and dependent claims 2-11, 13-18 and 20), the phrase -- to consult an accumulated failure rate real time function -- is vague, unclear, and indefinite. It is unclear how a function can be "consulted".

With regard to claim 9, the phrase -- a last square error -- is vague, unclear, and indefinite. A definition for a -- last square error -- has not been provided, which renders the claim indefinite.

With regard to claims 11, 18 and 20 the phrase -- while said testing time in which is corresponds by said testing time -- is awkward, vague, unclear, and indefinite.

With regard to claim 19, the phrase -- performing an optimizating process -- is vague, unclear, and indefinite.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyington et al. in view of Chien et al.

With regard to claims 1 and 12, Boyington et al. discloses providing a plurality of integrated circuits (col. 3, lines 31-33); performing a life-time testing process, wherein a failure rate testing time relation is established by measuring the life-time of each integrated circuit under a testing environment, wherein an acceleration factor is related to the relationship between a testing time of the testing environment and a real time of a normal operating environment [i.e., a core time is calculated from historical data (i.e., acceleration factor) which is the time of stress that is to be applied to all ICs in a batch]

(col. 3, lines 16-29); performing a transforming process using the acceleration factor function to transform the testing time function into a real time function, wherein a knee point of the real time function corresponds to an operation time which is a best burn-in time [i.e., when the failure slope (i.e., knee point) slows to a certain level, the determination is made that the infant mortalities have been identified and the remaining ICs need no additional burn-in (i.e., best burn-in time)] (col. 3, line 61 to col. 4, line 4, and col. 4, lines 8-23); and performing an integrating process by integrating a real time function through a calculating region to "consult" an accumulated failure rate real time function, wherein the calculating region is a region in which the real time is larger than the best burn-in time [i.e., a performance database is maintained that contains failure rates accumulated over a core period at read-points including a passing read-point (i.e., in order to determine a passing read-point, it is necessarily the case that the calculating region must extend beyond the best burn-in time)] (col. 3, lines 40-47).

Boyington et al. does not disclose simulating a failure rate testing time relation; or simulating a failure rate real time relation. Chien et al. discloses simulating a failure rate real time relation (page 463, "III. Methods" and "*B. Simulation*"). It would have been obvious to one of ordinary skill to modify Boyington et al. to simulate a failure rate real time relation that was transformed from a failure rate testing time function, and simulate a failure rate testing time relation, because Chien et al. teaches that by doing so, the total costs and the mean residual lives under different burn-in times can be calculated (page 463, "III. Methods"), and using either a testing time or real time relation are functionally equivalent in determining the results of the simulation.

With regard to claims 2 and 13, Boyington et al. discloses a failure rate testing time relation divided into three periods, infant mortality, normal, and wear out (Fig. 3 and col. 4, lines 5-8).

With regard to claims 3-8, 14 and 15, as noted previously, Boyington et al. discloses certain features of the claimed invention, including an acceleration factor function (i.e., core time, as noted previously; col. 3, lines 19-30) but does not explicitly disclose an acceleration factor function that is constant, linear, or nonlinear; or a testing time function that is an exponent function, a polynomial, or "$y=at^b$". Chien discloses an acceleration factor function that is constant, linear, and nonlinear; and a testing time function that is an exponent function, a polynomial, and in the form "$y=at^b$" (i.e., Equation (1) and Equation (3), which depending on the values of variables λ and β (i.e., "a") and "D" (i.e., "b"), will represent an acceleration factor that is constant, linear, and nonlinear, and a testing time function that is exponential, polynomial, and "$y=at^b$" (pages 462-463, "*A. U-Shaped Failure Rate Function*" and "*A. Generating a U-Shaped Failure Rate Curve*"), because failure rate is related to testing time and the acceleration factor function. It would have been obvious to one of ordinary skill to modify Boyington et al. to include an acceleration factor function that is constant, linear, and nonlinear; and a testing time function that is an exponent function, a polynomial, and "$y=at^b$", as taught by Chien, because Chien suggests that doing so allows the failure rate to be calculated in various regions of the failure rate curve including the constant failure rate region and the wear-out section (page 463, "*A. Generating a U-Shaped Failure Rate Curve*").

With regard to claims 9, 10, 16 and 17, as noted previously, Boyington et al. discloses minimizing an error (i.e., such as a last square error) between the failure rate testing time relation and the testing time function [i.e., dynamically fine tuning burn-in testing based on past performance data, such that the delta between instantaneous failure rates and actual read points is compared to established criteria in a performance database to dynamically control the duration of burn-in (i.e., the error between failure rates and the testing time function is minimized) (col. 4, lines 24-29 and 39-46).

With regard to claims 11 and 18, as noted previously, Boyington et al. discloses certain features of the claimed invention, but does not disclose stopping the integrating process when the testing time is located in the wear out period. Chien et al. discloses stopping the integrating process when the testing time is located in the wear out period.[i.e., "t_{L2}"is calculated (i.e., via an integration/summing process; (page 463, *A. Generating a U-Shaped Failure Rate Curve*) to determine when the product starts to wear out (page 463, "III. Methods")]. It would have been obvious to one of ordinary skill to modify Boyington et al. to stop the integrating process when the testing time is located in the wear out period as taught by Chien et al., because Chien et al. teaches that doing so allows a warranty plan to be set and a life-cycle model to be constructed (page 463, "III. Methods").

8. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyington et al. in view of Chien et al. and further in view of Matsuoka.

With regard to claim 19, Boyington et al. discloses providing a plurality of integrated circuits (col. 3, lines 31-33); performing a life-time testing process, wherein

the life-time of each integrated circuit is measured under a testing environment and a failure rate testing time relation is established in accordance with a plurality of testing records, wherein an acceleration factor is related to the relationship between a testing time of the testing environment and a real time of a normal operating environment, and performing an optimization process where part of the testing records are deleted and the process is performed again while more than one integrated circuit is failed [i.e., a core time is calculated from historical data (i.e., acceleration factor) which is the time of stress that is to be applied to all ICs in a batch (col. 3, lines 16-29); and the failure rate calculation which uses a failure rate testing time relation also considers statistical analysis of past performance data extracted from a performance database that enables burn-in testing to be dynamically fine-tuned (col. 4, lines 24-29); it is noted that Boyington et al. does not explicitly delete records, but rather a subset of prior records are used to optimize the determination of best burn-in time, which is functionally equivalent to the deletion of a portion of prior testing records/historical data]; performing a transforming process using the acceleration factor function to transform a specific testing time into a specific real time and transform a testing time polynomial into a real time polynomial, wherein the specific real time (i.e., a knee point of the real time function) corresponds to an operation time which is a best burn-in time for testing the integrated circuits [i.e., when the failure slope (i.e., knee point) slows to a certain level, the determination is made that the infant mortalities have been identified and the remaining ICs need no additional burn-in (i.e., best burn-in time)] (col. 3, line 61 to col. 4, line 4, and col. 4, lines 8-23); and performing an integrating process by integrating a

real time function through a calculating region to "consult" an accumulated failure rate real time function, wherein the calculating region is a region in which the real time is larger than the best burn-in time [i.e., a performance database is maintained that contains failure rates accumulated over a core period at read-points including a passing read-point (i.e., in order to determine a passing read-point, it is necessarily the case that the calculating region must extend beyond the best burn-in time)] (col. 3, lines 40-47).

Boyington et al. does not disclose simulating a failure rate testing time relation using a polynomial of the testing time; or determining a best testing time (i.e., bust burn-in time) of the integrated circuits while only one of the integrated circuits has failed before a specific testing time.

Chien et al. discloses simulating a failure rate real time relation (page 463, "III. Methods" and "*B. Simulation*"). Matsuoka discloses a monitored burn in system that has the capability of outputting an electrical signal when one of the integrated circuits fails, and calculating a cumulative failure rate, counting the cumulative number of failed integrated circuits at predetermined time intervals, and commanding burn-in to stop when a predetermined reference number of integrated circuits has failed (col. 3, lines 10-38).

It would have been obvious to one of ordinary skill to modify Boyington et al. to simulate a failure rate real time relation that was transformed from a failure rate testing time function, because Chien et al. teaches that by doing so, the total costs and the mean residual lives under different burn-in times can be calculated (page 463, "III. Methods"). Further, it would have been obvious to one of ordinary skill to modify

Boyington et al. to determine a best testing time (i.e., bust burn-in time) of the integrated circuits while only one of the integrated circuits has failed before a specific testing time (i.e., a predetermined reference count; col. 3, lines 27-32), because Matsuoka teaches that monitoring the burn-in process enhances the reliability of burn-in procedures (col. 1, lines 21-28).

With regard to claim 20, as noted previously, Boyington et al. discloses many features of the claimed invention, but does not disclose stopping the integrating process when the testing time is located in the wear out period. Chien et al. discloses stopping the integrating process when the testing time is located in the wear out period.[i.e., "t_{L2}"is calculated (i.e., via an integration/summing process; (page 463, *A. Generating a U-Shaped Failure Rate Curve*) to determine when the product starts to wear out (page 463, "III. Methods")]. It would have been obvious to one of ordinary skill to modify Boyington et al. to stop the integrating process when the testing time is located in the wear out period as taught by Chien et al., because Chien et al. teaches that doing so allows a warranty plan to be set and a life-cycle model to be constructed (page 463, "III. Methods").

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Moosa et al. discloses an accelerated life defect influence model relating the lifetime of an object to the defect magnitude of a defect in the object.

Leung, Jr. discloses a burn-in system that provides a cost-effective and reliable way to reduce the infant mortality of integrated circuits being tested and to estimate the longevity of the batch of integrated circuits from which they came.

Figal discloses that there are various ways to condense the stress period of a burn-in test into a shorter period of time so that a component does not have to be tested for 1,000 hours to see if it meets reliability requirements.

Chien et al. discloses a model to estimate optimal burn-in time and determine the optimal amount of redundancy for a subsystem.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy R. Stampf whose telephone number is 703-305-3339. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on 703-308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3431 for regular communications and 703-308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

trs
May 24, 2002

HAL WACHSMAN
PRIMARY EXAMINER
2857